Flight Computer for a Human Resources Training System in Small Satellite Technology*

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Abstract. A detailed description of a small, versatile and capable flight computer (FC) developed to automate the operations of a small satellite educative system (SES) is presented. The computer architecture was designed with the required hardware interfaces to allow the automation of a laboratory satellite educative system. However, in order to widen the applications of this computer, radiation protections were added to allow its use in real small space vehicles. In addition, the computer board was developed to accomplish with size and mechanical restrictions from cubesat picosatellites. The paper shows the SES global description, the flight computer architecture, the local sensors integrated, the buses that provide connectivity with other cards, the two layer PCB generated to save production costs and the validation software developed to test its hardware interfaces.

Keywords: flight computer, satellite educative system, portable equipment, training system, university technology.

1 Introduction

Our group is developing a cost-effective training system in small satellite technology employing commercial-off-the-shelf (COTS) parts from the automotive and services industries. The system was planned to be affordable enough to be used in laboratories with the intention to offer attractive, fast, and versatile training practices and courses in satellite technology and related fields. Our goal is to use the system in High Schools, Technological Institutes and Universities, with the intention of approaching young people to the world of space applications, Science and Technology.

In addition, the SES will also be useful in research laboratories to develop new solutions and modules for real satellite subsystems. In this sense research in fields such as three axis stabilization, digital communications, satellite sensors, power systems, payload validation, flight computers, navigation autonomy, and satellite constellations, would also be addressed with the support of this laboratory tool.

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It must be mentioned that commercial availability of similar products to the SES is rarely seen in the global market. Right now the only satellite educative commercial product detected by the authors is the Eyassat educational system developed initially by the US Air Force and commercialized by Colorado Satellite Services, [1]. Besides, we found that few institutions have developed their own satellite prototypes to accomplish laboratory research in distributed space systems, as the case of the Israel Institute of Technology [2] and the case of the US Naval Academy Satellite Laboratory with its "LABsat" experimental hardware, [3]. The Eyassat basic equipment starts at 8,000 dollars. However, this price is difficult to be afforded in developing countries. This is why the SES is planned to be developed and offered for under 3,000 US dollars cost in order to be attractive for different schools, universities, and so on. This goal shaped the design and the main characteristics of the SES in order to achieve a cost-effective development.

It is also important to highlight that we are taking advantage of previous experiences in space projects, [4], [5] and [6], to fast track this project.

1.1 Further Applications of SES Computer

With the intention to increase the applications of the SES flight computer generated by our group, we planned to use it also in 1 kg picosatellites, like the one we are informally developing in our laboratory. Once the SES Project gets finished and the required documentation with CONACYT gets accomplished our goal is to start the picosatellite project.

1.1.1 Some characteristics of picosatellite missions

The cubesat picosatellite concept was developed by Dr. Robert Twiggs from Stanford University in 1999, [7]. Since then a great amount of universities from all over the world are developing, planning to build, or have developed a picosatellite project to enter the space activities. Among the countries involved in CubeSats projects are: USA, Canada, Germany, Japan, Denmark, Netherlands, Norway, Switzerland, Australia, Korea, Malasya, Argentina and Colombia, [8]. The last, through the "Universidad Sergio Arboleda", launched successfully the picosatellite called "Libertad 1" the 17th April 2007, [9].

The cost of this type of projects depends on the country that makes it as well as in the payload, and go from <100,000 to 1,500,000 US dollars including the costs of inception, launch, operation and end-of-life.

The picosatellite missions are launched in groups as secondary payloads on rockets from different countries. However, Russian rockets are often selected for launching purposes because of its attractive cost (40,000 US dollars in 2006). On the other hand, there are a couple of companies in USA that commercialize the fundamental subsystems to construct a picosatellite. They charge 6,000 US dollars for every subsystem such as: structure, communications, electrical power, attitude determination & control, and flight computer. Nevertheless, it is important to notice out that additional investment has to be considered for experiments, development of operations software, environment tests, launching services and ground station.

Furthermore, it has to be taken into account that low-earth-orbit picosatellite missions have a typical lifespan of 3-9 months. In addition, it should be highlighted that picosatellite missions are attractive and demanded around the world because they are employed for technology demonstrations, proof-of-concepts, scientific experiments and human resources training, [10], [11]and [12].

2 Architecture of the satellite educative system

The SES is basically formed by a laboratory satellite prototype (LSP), operations software for LSP, and a laptop with executable software to monitor and control the LSP, figure 1. The last contains what is referred as the Ground Station Software (GSS) for Telemetry acquisition and Command Shipment.

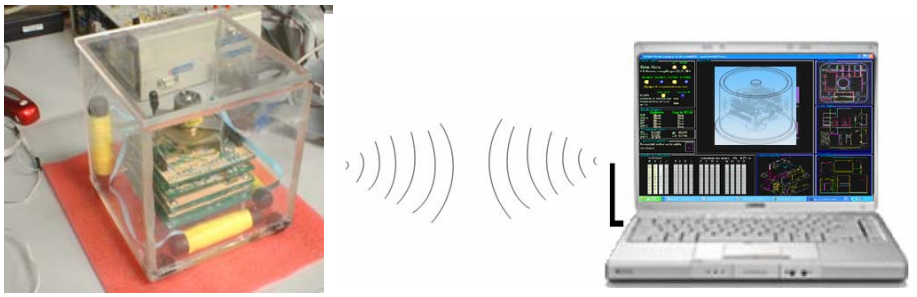


Figure 1. The satellite educative system, on the left side the LSP mockup at real scale is shown.

3 The flight computer subsystem

The LSP has a single board flight computer (FC) with lateral connectors employed as electrical buses to interconnect electronic cards in tandem. The electrical connector offers mechanical attachments among printed circuit boards. In addition, each PCB contains holes at each corner to screw the whole printed board array to the LSP structure.

With the use of bus type connectors all the electrical signals from the flight computer are available for all the assembled cards, thus it is possible to interconnect cards without caring the order of them. Besides, it is important to notice out that all the bus type connectors in the cards are female type in the top side, whereas the bottom side is a wire-wrap connector. This allows the interconnection of cards in tandem either by the top or by the bottom sides.

The PDS single board computer is built around the 16 bit RISC SAB80C166 processor from Siemens with extended temperature (see figure 2), 40 Mhz oscillator, 256 kb of RAM memory where the SES operations software will be loaded, figure 3, hardware for automatic uploading of new programs to the flight computer, two main serial ports and 8 extended serial ports generated by multiplexing the second main serial port. The serial ports support full-duplex asynchronous communication up to 625 Kbaud and half-duplex synchronous communication up to 2.5 Mbaud.

On the other hand, the 100-pin SAB80C166 microcontroller internally contains important resources as follows: a watch dog timer, interrupt controller, 16-bit timers, 10-channel 10-bit A/D converters, two serial channels and several 16 bits I/O ports, with a total of 76 I/O lines.

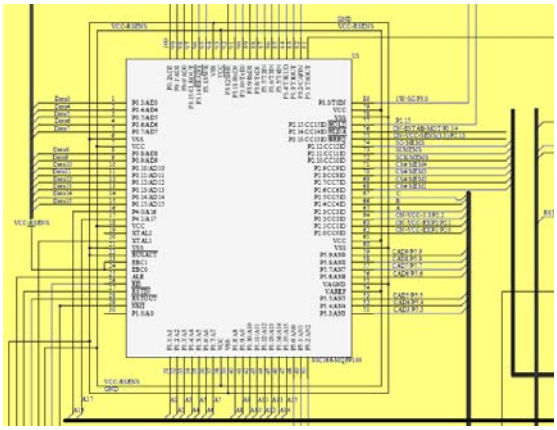


Figure 2. FC is based on a 16 bit RISC Siemens microcontroller.

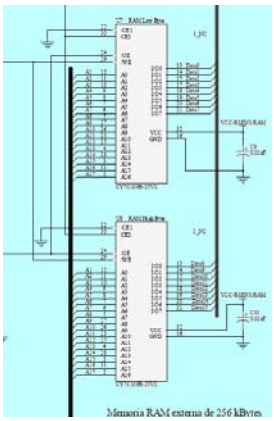


Figure 3. FC contains 256 Kb of SRAM.

The main specifications for the flight computer are the followings:

- 8.9 x 8.9 cm printed circuit board,
- Two layer PCB for easy and cheap fabrication,
- 16 bit RISC microcontroller, SAB80C166 from Siemens,
- Microcontroller PIC16F876A to control the process of new software uploading to the SAB processor,
- 256 Kb of SRAM for program execution,
- 32 Mb of Flash RAM for massive data storage,
- SPI port emulated with I/O lines and dedicated software,
- 3 local 1-wire temperature sensors,
- 3 local 1-wire current sensors,
- Latch-up protection for main resources from FC such as: SAB80C166 processor, SRAM and PIC16F876A,
- Multiplexing module to generate 8 extended serial ports to the SAB80C166 processor for communications with other boards from the satellite educative system.

3.1 Flash memory for massive data storage

The flight computer contains 4 AT45DB642D flash memories to offer a whole storage capacity of 32 Mb, each flash memory has a storage capacity of 8 Mb. The flash memories are accessed by SPI interface through 4 communications lines connected to the SAB microcontroller. The technical specifications for the AT45DB642D are the followings:

- Voltage supply from 2.7 V to 3.6 volts.

- SPI interface up to 66 MHz.
- 8 Mb Flash memory organized in sectors of 256 Kb, blocks of 8Kbytes and pages of 1 Kb.
- Two SRAM buffers each one of 1 Kb.
- Operation Temperature from – 40 °C to + 85 °C.

Besides, it was developed a LabVIEW software to validate the programming and operation of Flash memories in laboratory. For this purpose a 1 layer PCB was developed in the laboratory to solder the surface mount flash memory. This process allowed the early validation of programmed software related to the Flash memories. Figure 4 shows the schematic diagram of the flash memory module while figure 5 shows the software interface employed to access the memories in laboratory.

3.2 Sensors installed on board the flight computer

The 1-wire sensors from the automotive industry are attractive because they are cheap and enable important reductions of line tracks in the PCBs and also reduce the amount of interconnection wires between system boards. Moreover, the 1-wire sensors let a microcontroller device to access an important amount of sensors by means of only two wires. This contrasts with conventional sensors, which require two wires for each included sensor.
By these reasons, the flight computer is instrumented with local sensors that are intended mainly to use the FC in a Picosatellite mission. However, the sensors will also be of important use in the satellite educative system to show the user the applications and importance of telemetry systems. In addition, the sensors will make possible the interactions among user and SES to modify directly the readings of temperature sensors when they be touched, by instance, by the user´s finger.

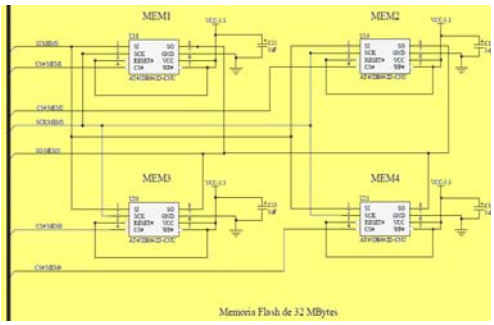


Figure 4. Schematic circuit of the Flash memory module.

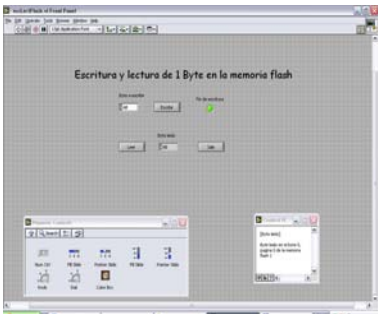


Figure 5. LabVIEW software developed to validate basic operations with Flash memories.

The FC has three DS18S20 1-wire temperature sensors. The three sensors are connected to the same input port from the SAB controller. The 1-wire temperature sensors have the following specifications:

- Every sensor has a unique ID serial number of 64 bits called ROM Code.
- Supply voltage from 3.0 V a 5.5 V.
- Temperature measurement from - 55 °C to + 125°C.
- ± 0.5 °C precision in the interval from – 10 °C to + 85 °C.
- 9 bit resolution.

- Temperature A/D conversion time of 750 ms (max.).

In order to validate the software programming for the temperature sensors a LabVIEW software was developed. Figure 6 shows the presentation of results with this software.

3.3 Operations Software for the flight computer

The LSP will contain an operations control software loaded in the flight computer to carry out the following functions:

- Communications with the laptop software,
- Command requests from GSS,
- Reception and execution of new programs of up to 256 Kb,
- Acquisition, packing, data storage in flash memory, and transmission of telemetry by wireless means,
- Managing of protocols with GSS,
- Simulation of orbital times for LSP,
- Real time operations with LSP,
- Communications with SES subsystems (stabilization, power, digital audio and payload) through digital commands,
- Data acquisition of local sensors, among them: 3 1-wire temperature sensors and current sensors associated with latch-up sensors (SAB80C166, SRAM and PIC16F876A),
- Activation and deactivation of SES subsystems through the help of the power subsystem. This feature allows the system to save energy from the batteries,

Regarding the software development for the SAB80C166 it is written in standard "C" language, programs are compiled using the BSO Tasking family of tools for the SAB80C166 microcontroller.

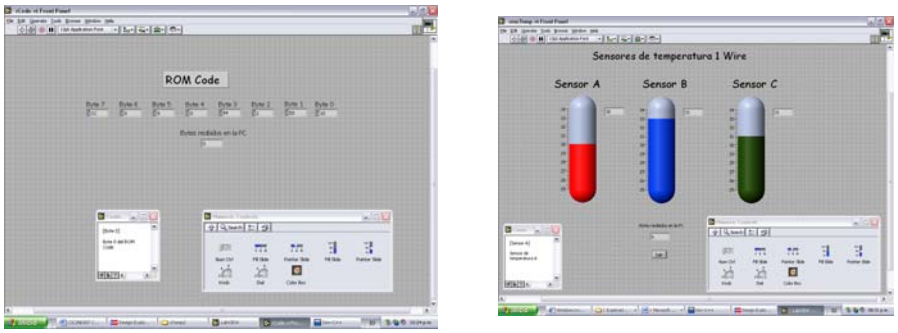


Figure 6. LabVIEW software employed to display the ROM code and the temperature of the three 1-wire temperature sensors from FC.

4 Latch-up effect protections

Considering that the flight computer will be used as well in picosatellites to be launched into space orbit, the flight computer design includes hardware protections to prevent the destructive latch-up effect generated by cosmic radiation. This

phenomenon affects electronic parts when they are taken to space orbit. The latch-up prevention hardware was installed in those components with higher possibilities to be affected, in this case the electronic parts with higher integration scales and associated to most important computer resources. Therefore these protections were placed in the SAB80C166 16 bit RISC microcontroller, its 256 Kb of external SRAM (from where the FC programs are executed) and the PIC16F876A (which controls the up-loading of new programs to the Siemens microcontroller).

The protection detects the electrical current consumption for every device and automatically generates a digital output pulse when any one of them reaches a maximum allowed current threshold level. These signals are taken to the lateral connectors and will be captured by the picosatellite power subsystem board. This subsystem will process the signals pulses and will turn off the power supply for the alarmed subsystems. This is the only mechanism that can stop the destructive latch-up effect.

The latch-up circuit placed in the FC is formed by the MAX4071 (current to voltage converter) and the LM6511 (voltage comparator), figure 7.

In addition, an A/D DS2450 1-wire converter device was placed between the MAX4071 and the LM6511. The 1-wire voltage sensor will be used by the SAB80C166 to collect telemetry data from latch-up current sensors. The voltage sensor has the following specifications:

- 1-Wire interface,
- 64 bit ID number for every device,
- 4 A/D converters per chip,
- 16 bit resolution,
- 5V voltage supply,
- Operating temperature from – 40 °C to + 85 °C.

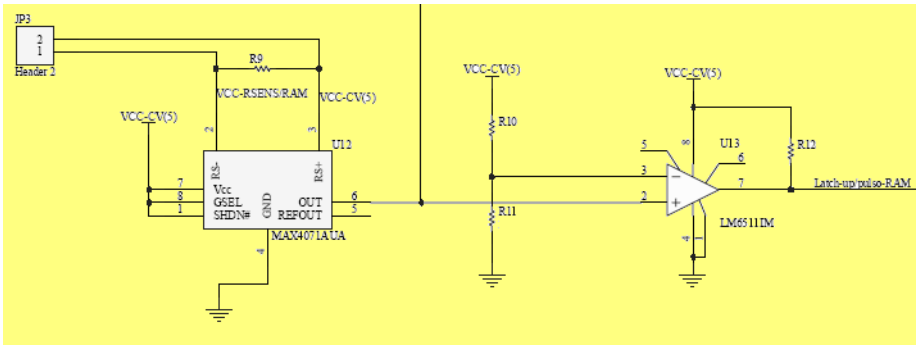


Figure 7. Latch-up protection circuitry for SRAM.

4.1 Latch-up current measurements

An additional LabVIEW software was developed to validate the basic operations of FC current sensors. This performs the programming and data reading of 1-wire current sensors. Figure 8 shows the graphical interface of the software, as can be seen the visualization of results is simple and straightforward. Validation tests were

successfully performed in laboratory with this software and electronics assembled in 1 layer temporal PCB.

It is important to highlight that the flight computer PCB will be the same for both the SES and Picosatellite missions. However, the protection components will be installed exclusively in computers elaborated for Picosatellites. In other words, the SES computers will not install these electronic parts because they will be employed in terrestrial environment. The goal is to employ the same PCB computer for both applications to lower the development cost of our small satellites projects.

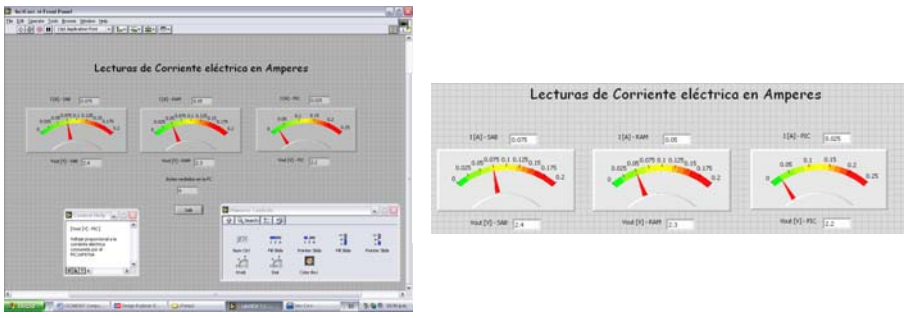


Figure 8. LabVIEW interface developed to validate the programming and operation of FC current sensors.

5 Uploading new programs to the flight computer

The versatility and friendly operation of the satellite educative system will depend, among other things, on its flexibility to upload new programs to the LSP. This feature will allow the user to make changes, studies, practices and research activity with the educative system. Unfortunately, the SAB80C166 needs external control in order to achieve this operating mode. By this reason, a PIC16F876A microcontroller was added to the design. This processor is programmed to read the GSS serial port and continuously looks for the detection of the "upload new program" command. Once this is detected the PIC controller frees the communication channel among GSS and SAB80C166 and drives control signals from the SAB80C166 (ALE and NMI).
This process allows the SAB processor to execute its internal boot ROM which contains communications software to detect the baudrate speed and to receive the new software by serial port. This process takes three different steps, in the first one the SAB device receives a 32 byte program in its internal RAM and automatically executes it. This program allows the uploading of a second program of 256 bytes. The third step allows up to 256 Kb of software to be uploaded in the FC external SRAM. Every step is monitored by the PIC16F877 microcontroller, whenever the process is successfully concluded the PIC resets the SAB device in order to start automatically the execution of the new program with full control form the SAB processor.

In order to validate the new program uploading function for the flight computer LabVIEW software was developed. It allows the opening of a file with HEX extension and sends it through serial port. Considering that the FC board is not yet ready for testing, the uploading software was tested with a SAB80C166 card developed in our lab for a previous project, figure 9. The software performed without

problems and is ready for FC laboratory testing once the board is ready for assembly and testing. The LabVIEW software is shown in figure 10.

6 PCB design and fabrication

The two layer printed circuit for the flight computer board was elaborated with Protel DXP software, a powerful tool for design and manufacture of printed circuits boards. It allows the use of different data bases for components as well as the creation of new components and the possibility to aggregate them to the project. It also enables the positioning of components and the automatic routing of connections between the components of the project in a very short time and in an efficient way.

Figure 9. Electronic board employed to validate the uploading software.

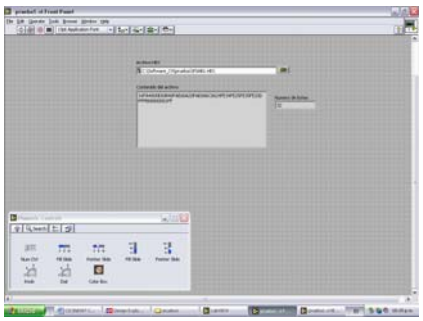
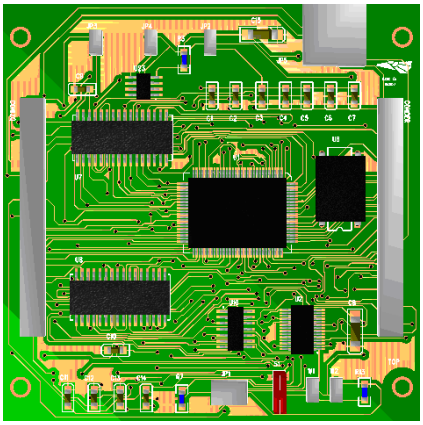


Figure 10. LabVIEW software developed to send new programs to the flight computer.

To elaborate the FC several component distributions on the board were practiced to allow the full automatic routing of the PCB. In our case the distribution is very important because the FC architecture includes many electronic components, most of them of surface mount type and few of them of dual in line type. However, the PCB area is too small to allocate the components in a suitable way to admit the automatic routing of electrical lines. This is the reason by which several chosen component distributions never reached the auto-routing completion. The final and successful distribution is shown in figure 11. This design is to be sent for manufacture in the next weeks, once this becomes manufactured, basic revision will take place and then parts assembly and partial testing will be applied.



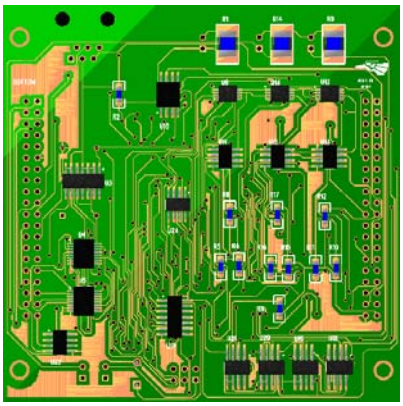


Figure 11. Flight computer PCB ready for manufacturing process.

7 Concluding Remarks

We have presented the FC computer design, the global architecture, the preliminary tests performed with dedicated software specially developed for this purpose and the PCB development process. Few hardware interfaces such as 1-wire sensors, latch-up protection and new program uploading, required preliminary tests to validate the designs. This work will increase the success chances to generate an operative PCB from the first manufacturing run.

In this way, the final flight computer PCB is ready to be manufactured. We expect to have it ready in few weeks to proceed with its assembly and progressive testing in order to reach an operative flight computer by the end of 2007.

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